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HANDBOOK OF VLSI ROUTING TECHNIQUES:

SERIAL AND PARALLEL MODELS

超大规模集成电路布线技术

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Professor Pinaki Mazumder received his PhD in Electrical and Computer Engineering from the University of Illinois at Urbana–Champaign in 1988. Prior to that, he received his MS degree in Computer Science from University of Alberta in Canada, BS degree in Electrical Engineering from Indian Institute of Science at Bangalore, and BSc Physics Honors degree from Guwahati University in India. Currently, he is a Professor of Electrical Engineering and Computer Science at the University of Michigan where he has been teaching for the past 25 years. He spent 3 years at National Science Foundation serving as the lead Program Director of Emerging Models and Technologies Program in the CISE Directorate as well as leading the Quantum, Molecular and High Performance Simulation Program in the Engineering Directorate. He had worked for 6 years in industrial R&D laboratories which included AT&T Bell Laboratories in USA and Bharat Electronics Ltd. in India. Professor Mazumder spent his sabbatical at Stanford University, University of California at Berkeley, and NTT Center Research Laboratory in Japan. He has published over 260 technical papers and 4 books on various aspects of VLSI technology and systems. His research interest includes CMOS VLSI design, semiconductor memory systems, CAD tools and circuit designs for emerging technologies including quantum MOS, spintronics, plasmonics, and resonant tunneling devices.

Professor Mazumder's inventions in testable DRAM circuits, in-line accelerated testing procedures for high-density RAM chips, and testing of embedded ROM and SRAM through JEDEC boundary scan ports are widely used by memory and FPGA manufacturers. His research in biology-inspired VLSI layout synthesis, self-healing VLSI design and self-repairable memory compilers has made commercial impact. In revolutionary emerging technologies, Professor Mazumder has made sustained impact for the past 20 years by collaborating with multiple leading researchers in universities and companies. His research group has developed a Quantum SPICE simulator to design several innovative quantum tunneling based circuits that were fabricated by many US companies. Professor Mazumder was a recipient of Digital's Incentives for Excellence Award, BF Goodrich National Collegiate Invention Award, and DARPA Research Excellence Award. Professor Mazumder is an AAAS Fellow (2007) and an IEEE Fellow (1999) for his distinguished contributions to the field of VLSI.

Pinaki Mazumder教授是IEEE Fellow和AAAS Fellow，密歇根大学安娜堡分校（University of Michigan, Ann Arbor）工学院电气工程与计算机科学系的终身教授。1988年，Mazumder教授开始研究电子设计自动化（EDA），并在密歇根大学开设研究生课程VLSI Layout Algorithms（EECS627，超大规模集成电路布局算法），至今已在EDA领域耕耘30余载，共发表100多篇顶级期刊/会议论文，出版四本专著。

本书是Mazumder教授的扛鼎之作，既汇集了EDA领域“大家”的重要成果，也涵盖了EDA领域包括作者及其团队在内的研究者的最新成果，聚焦超大规模集成电路布线技术，从串行与并行布线模型开始，研究迷宫布线算法、总体布线算法、详细布线算法（即通道布线与开关盒布线算法等）和特殊布线算法，兼顾芯片设计中的特定情况，重点讨论了工业界使用的大量特殊类型布线技术与最新的并行布线器，具有较高的通用性和实用性，有望推动超大规模集成电路布线工具的持续发展。

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Preface

This handbook for routing interconnects inside a VLSI chip provides mathematical models of important classes of wiring techniques for students interested in gaining insights in integrated circuits layout automation techniques and for practicing engineers working in the field of electronic design automation (EDA). This book presents a comprehensive review on VLSI routing techniques that was undertaken in early 1990's with a view to developing a generalized routing accelerator that could speed up routing chores for different styles of wiring techniques, namely, *maze routing* used widely for connecting different circuit blocks by finding the shortest path, *channel routing* used in connecting standard cells of uniform heights and variable widths arranged in the form of rows of cells, *switchbox routing* used in connecting surrounding multiple blocks of dissimilar aspect ratios within an enclosed routing area, and so on.

In 1988, when I started my academic career at the University of Michigan, I designed a new graduate-level course on computer-aided design, EECS 527: VLSI Layout Algorithms. The course was introduced to educate graduate students and spur doctoral research in the-then burgeoning field of computer-aided design (CAD) for integrated circuits (ICs) that propelled the exponential growth of integration density in VLSI chips, as postulated by Moore's Law. At that time, there was no suitable textbook on the subject to teach graduate students about the state-of-the-art layout algorithms that were key to design complex VLSI chips. Therefore, I combed through the literature on the subject and assembled the course materials in order to teach students systematically basic underlying mathematical techniques for circuit partitioning, floor-planning, cell placement, and routing. Subsequently, I engaged my own doctoral students to expand my lecture materials in the form of comprehensive reviews.

For example, with the assistance of my doctoral student, Dr. K. Shahookar, who studied the Genetic Algorithm (GA) for VLSI cell placement techniques, I coauthored a 78-page review paper, which was published in *ACM Computing Surveys* in June 1991. After poring over nearly a hundred publications on placement algorithms for standard cells and macro-cells, I divided them into five main categories: (i) the placement by simulated annealing, (ii) the force-directed placement, iii) the placement by min-cut graph algorithms, (iv) the placement by numerical optimization, and (v) the evolution-based placement. While the first two types of algorithms owe their origin to physical laws, the third and fourth are analytical techniques, and the fifth class of algorithms is derived from biological phenomena. The taxonomy of placement algorithms was created to study inherent parallelism of the different classes of algorithms. While designing the course, I realized that in order to push the mammoth potential of Moore's Law, the chip design phase must be accelerated several folds by harnessing the evolving computing platforms.

In the late 80's, the computing platforms for the VLSI design environment were rapidly transforming from mid-frame computers, namely, Digital Equipment Corporation Vax 11/780, Hewlett Packard HP 3000, and Wang Laboratories Wang VS, to the network of workstations, what is widely known as the NOW. This opportunity in hardware evolution warranted deeper insights into VLSI cell placement and routing (P&R) techniques so that sequential algorithms that used to run on standalone mid-frame computers could be rendered into parallel CAD algorithms for running efficiently on the NOW platform. Also, emergence of commercial parallel

computers such as Intel hypercube and Sequent Computer System shared memory had further pushed the needs for developing parallel P&R algorithms.

In order to promote the NOW platform for EDA research, I started working with my students to develop imaginative distributed Genetic Algorithms (GAs) for partitioning, placement and floor-planning techniques needed in VLSI chip layout automation. My research group had at that time developed an EDA tool, named *Wolverines* for parallel implementation of standard cell placement algorithms on the NOW platform. Since workstations are connected by a local area network (LAN) that often deploys the Ethernet to connect different workstations, communication of packets between two specific workstations generally require considerable time even when the Ethernet did not undergo collision of message packets. Because of the length of a LAN, two workstations located afar may locally sense and infer that the Ethernet is free and may launch packets asynchronously. In case, there is a collision of packets, all the senders must abandon transmission by backing off. Then they wait randomly within the range of time before attempting to transmit the packet. If a sender encounters the collision of packet again, it then waits randomly over a period of time that is twice longer than the previous time period. This exponential backing off protocol used in random-access LAN causes a severe constraint to run parallel routing algorithms because of their fine-granularity of parallelism in contrast with placement algorithms that do not require frequent communications in parallel mode of operation over the NOW.

Therefore, the vision I had at that time is to develop distributed version of Genetic Algorithms (GAs) that can accelerate the partitioning, floor-planning and placement of cells on the NOW without requiring any hardware augmentation of workstations. The main impediments we encountered at that time were that unlike simulated annealing and graph-based techniques, the GAs could not be directly applied to solve VLSI layout problems. Professor John Holland, who invented the Genetic Algorithm at the University of Michigan, had devised the GA to solve a plethora of theoretical and practical problems that quintessentially required *functional optimization.* The GA applies its biology-inspired operators such as crossover, mutation and inversion in the genotype or chromosomal representation of the problem. The fundamental premise in GA is that genetic codes of biological creatures encapsulate their physical characteristics. The crossover operator in the GA produces offspring by splicing fragments of two different chromosomes pertaining to the two parents. Therefore, the GA applies all its transformations by combining the features of chromosomes on the genotype of a problem. In order to obtain the solution of a problem, the genotype is mapped on to its phenotype or physical appearance. It is well known that the functional optimization problems work very well with GA type algorithms since there are no inconsistencies between the genotype and phenotype of a problem. In other words, the genetic codes always generate feasible solutions in functional optimization problems.

However, the EDA algorithms for placement is a *constrained combinatorial optimization* problem where the genotype and phenotype must be carefully handled to ensure that all the cells are included in the phenotype and there are no duplication of cells. Traditional crossover operator used in the GA may produce infeasible solutions, unless before the application of each crossover operation pre-processing of the chromosome is performed carefully. In my book, *Genetic Algorithms for VLSI Design, Layout and Testing*, Prentice Hall, 2000, coauthored with

Dr. Elizabeth Rudnick, we have discussed Order Crossover, PMX Crossover and Cycle Crossover operators to eliminate infeasible solutions. However, we discovered that they incur significant timing overhead as the entire pair of chromosomes has to be scrutinized and evaluated to generate new offspring. These issues become very unwieldy as the problem size increases with the scaling of VLSI chips and may require a suboptimal divide-and-conquer strategy to strike a tradeoff between run-time and the solution quality.

Further, such improved crossover operators work for only the permutation class of problems such as standard cell placement techniques. The GA book discusses a refined version of the standard cell placement technique, called Simulated Annealing and Genetic Algorithm (SAGA) to improve the quality of cell placement solution. The algorithm runs like genetic algorithm initially to rapidly converge to a solution very close to the global optimization. And, then it slowly morphs into simulated annealing by increasing the mutation rate that iteratively applies random displacement of a single cell, instead of movements of multiple cells associated with the crossover operation. For macro-cell placement, the book discusses multidimensional compact crossover operators that can be innovated by using complex data-structures used in Heapsort algorithms. The book also shows how GA based EDA tools can be implemented on a network of desktop workstations to run super linearly while accruing the solution quality comparable to the ones achieved by running on a standalone processor. Especially, we studied different topologies of virtual sockets such as star, ring and hypercube between different workstations. We also experimented with the rate of communications (epoch) between different workstations to improve the quality of solution. From these various experimental results on a suite of benchmark circuits and comparing them with the results obtained by using cutting-edge EDA tools, we demonstrated that the GA has intrinsic parallelism mechanisms that can be cleverly exploited to develop parallel EDA tools for cell placement, which run efficiently on the NOW platform.

However, the VLSI routing algorithms such as maze, switchbox and channel routings require fine-grained parallelism that cannot be accomplished on a LAN because of uncertain delay associated with workstation-to-workstation communications. In order to support fine-grained parallelism in maze routing several special-purpose hardware such as NTT Adaptive Array Machine, IBM Wire Routing Machine, Waseda University Toroidal Machine, and University of Southern California L-Machine were built. In our maiden effort to develop hardware accelerator for maze routing, my research group had built the Hexagonal Array Machine that could support three-dimensional routing by concurrently propagating waves over multiple layers. Unlike the 2-D maze router that propagates waves from 4 neighbors of a base cell, the HAM propagates from 6 neighbors that include a grid point in the upper layer and another in the lower layer. Therefore, HAM finds the shortest path that may meander through multiple layers, if a path exists. Therefore, this feature of HAM reduces the need for rip-up and rerouting, as frequently demanded by 2-D maze routers due to the greedy nature of the maze search algorithm.

After realizing the key limitations of such dedicated routing accelerators that could only speed up the maze routing, my student, Dr. V. Ramachandran, who is the coauthor of this book, started looking into the possibility of developing a unified routing fabric that can be utilized to accelerate all sorts of VLSI routing algorithms. In his doctoral work, he proposed a polymorphic

architecture that mainly comprises an ensemble of simple processing elements that can be configured into various connection topologies by including a suite of switches in each processing element. The highly parallel single instruction multiple data (SIMD) architecture is generally known as Content Addressable Array Parallel Processor (CAAPP) and has been originally developed for image processing applications. Specifically, Dr. Ramachandran had used the CAAPP software framework to experiment with the virtual polymorphic hardware fabric, on which different types of routing algorithms including maze, channel and switchbox were mapped as reported in Section 5.3 in this book.

My overall vision in EDA was to develop distributed networks of workstations furnished with specialized hardware accelerator board containing the polymorphic chip to accelerate different styles of VLSI routing algorithms, while Genetic Algorithms will speed up the cell placement algorithms. Due to funding constraints, in our research group we could fabricate a tiny proof of concept polymorphic chip as shown below. The purpose of this handbook is not only to introduce different styles of VLSI routing algorithms, but also to exposit the ramifications of hardware-software co-design for such fine-grained parallel algorithms over a polymorphic fabric so that various types of chip routing algorithms can be accelerated, while the placement and floor-planning algorithms will be speeded up by leveraging the intrinsic parallelism of genetic algorithms. With this vision in mind, I hope that readers will be motivated to advance the frontiers of VLSI chip design through innovating hardware-software co-design methods as espoused in this routing handbook.

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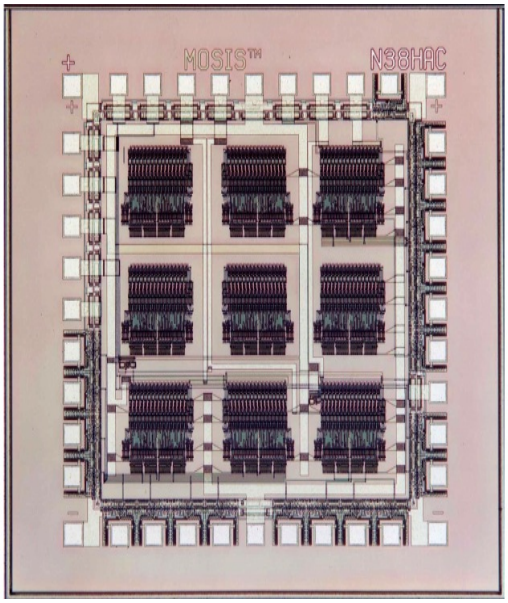

VLSI Routing Accelerator using Polymorphic Architecture
Designed and Fabricated by Ramachandran and Mazumder